

Memory Scheduling for Modern Microprocessors

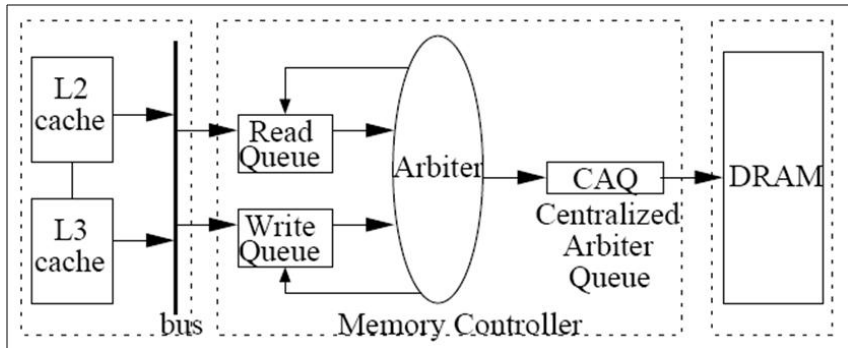
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- 1 Motivation
 - Architecture
- 2 Previous Techniques
 - Historyless
 - In-order
- 3 Adaptive History Based (AHB) Scheduler
 - How AHB Works
 - Scheduler Selection Logic
 - Benefits

Why Schedule Memory?

- Reduce Latency
- Increase Throughput
- Prioritize Memory Operations
- Avoid Bottlenecks in memory access

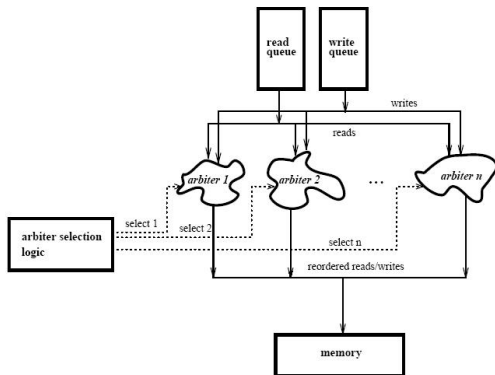


Historyless

- The read and write queues hold instructions that cause bank conflicts -HOLD.
- FIFO scheduler.
- Gives priority to reads.

In-order

- The read and write queues do not hold instructions that cause bank conflicts. Instead they are sent to the Centralized Arbiter Queue (CAQ) -NOHOLD.
- FIFO scheduler.
- Reads and writes have equal priority.



Scheduler Selection Logic

- 1 Uses number of reads, number of writes, and period of adaptivity.
- 2 Analyzes the memory command pattern.
- 3 Probabilistically selects the optimization criterion.

Benefits of AHB

- 1 Allows the scheduler to better reason about delays associated with its decisions.
- 2 Provides a mechanism for combining multiple constraints (helps account for increasingly complex DRAM structures).
- 3 Avoids certain bottlenecks in the memory controller by selecting operations that maximize a programs mixtures of reads and writes.